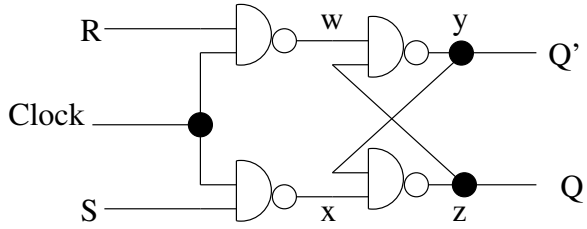
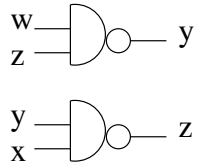
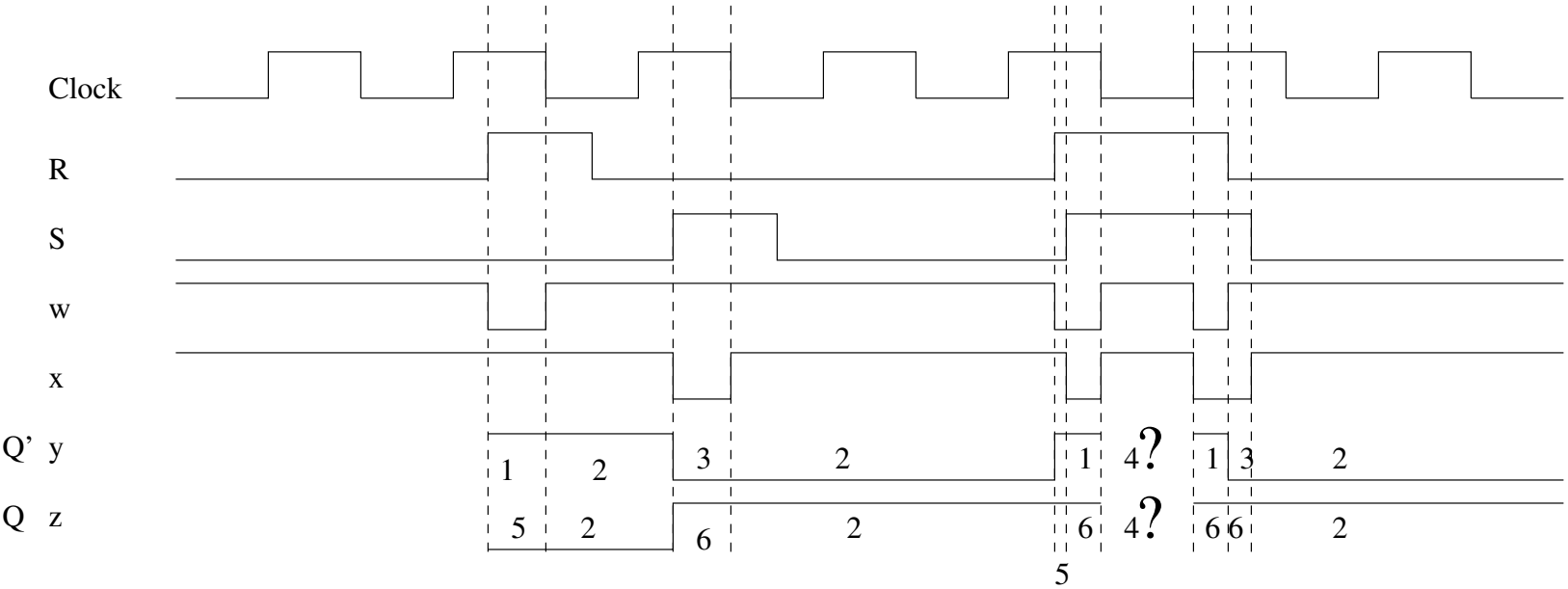



| a b | NAND |
|---|---|
| 0 0 | 1 |
| 0 1 | 1 |
| 1 0 | 1 |
| 1 1 | 0 |

When clock = 0, w=1.
When clock = 1, w=R'
When clock = 0, x=1.
When clock = 1, x=S'

When a=1, NAND output = b'
When a=0, NAND output = 1






1: w=0, forcing y=1
2: w=1, x=1, so y=z' and z=y', no problem, since y and z have opposite values
3: w=1, so y=z'
4: w=1, x=1, so y=z' and z=y', but there is a problem: both y and z have the same value! So it's undetermined what values y and z have.
5: x=1, so z=y'
6: x=0, forcing z=1

This is technically a latch, since it changes the value at Q when Clock = 1